AMENDMENTS TO THE CLAIMS:

Please amend claim 34 as follows:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. *(Cancelled)*

2. *(Previously Presented)* An integrated circuit for use as a scheduler of activities to be run on an associated processor, being of modular structure and constructed from an assembly of tiles, wherein each tile defines a building block having logic and structure, said tiles being abutted one against the other to form a two-dimensional array of n rows and m columns which realizes an overall functionality for the integrated circuit and wherein each of the 'n' rows of tiles provides the control logic for each one of 'n' schedulable activities and each of the m columns of tiles provides a particular function.

3. *(Original)* An integrated circuit as claimed in claim 2 comprising a further row of tiles for interfacing with an associated central processor and for generating control signals for said two-dimensional array.

4. *(Previously Presented)* An integrated circuit as claimed in claim 2 in which the control logic includes means for holding control variables corresponding to each of said

activities and next-activity selection logic for identifying those activities which are ready for running on the processor, depending on the status of said control variables.

5. *(Original)* An integrated circuit as claimed in claim 4 in which the control variables include at least one "stim-wait" channel.

6. *(Previously Presented)* An integrated circuit as claimed in claim 2 including means for setting those control variables comprising a "stim-wait" channel in response to a signal received from an associated processor.

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7. *(Previously Presented)* An integrated circuit as claimed in claim 2 including means for setting those control variables comprising a "stim-wait" channel in response to a signal received from an associated peripheral device.

8. *(Previously Presented)* An integrated circuit as claimed in claim 2 including means for setting those control variables comprising a stim-wait channel in response to a signal received from a second integrated circuit.

9. *(Previously Presented)* An integrated circuit as claimed in claim 2 including means for temporarily inhibiting any changes to control variables from entering the next-activity-selection logic.

10. *(Previously Presented)* An integrated circuit as claimed in claim 2 and incorporating decoding and encoding logic for routing signals, identifying one or more of said 'n' activities, between the associated central processor and the appropriate row of tiles.

11. *(Previously Presented)* An integrated circuit as claimed in claim 2 in which the next-activity-selection logic includes means for selecting the next activity to be run on a round robin basis.

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12. *(Previously Presented)* An integrated circuit as claimed in claim 2 in which the next activity selection logic includes means for allocating differing priority levels to groups of activities, and for selecting the next activity to run within a group on a round robin basis within that group.

13. *(Previously Presented)* An integrated circuit as claimed in claim 2 and including means for detecting when a schedulable activity has a higher priority than that activity currently running on an associated central processor and thereby generating an interrupt signal.

14. *(Previously Presented)* An integrated circuit as claimed claim 2 and incorporating a counter circuit.

15. *(Previously Presented)* An integrated circuit as claimed claim 2 configured for asynchronous operation, by incorporating level-driven, clock-free ripple logic.

16. *(Previously Presented)* An integrated circuit as claimed in claim 2 and being fabricated using CMOS techniques.

17. *(Previously Presented)* A processing network responsive to an activity scheduler as in claim 22.

18. *(Previously Presented)* A processing network as in claim 17, further comprising at least one peripheral device for setting at least one control-variable in said integrating circuit.

19. *(Previously Presented)* A multiprocessor network comprising a plurality of processors, each responsive to an activity scheduler as in claim 22, wherein the activity schedulers are linked together.

20. *(Cancelled)*

21. *(Cancelled)*

22. *(Previously Presented)* An activity scheduler arranged to control activities in a processor, comprising:

an integrated circuit to support data and multi-tasking for the processor,

the integrated circuit being configured to support a control node mechanism comprising a set of stim-wait channels,

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the integrated circuit further incorporating next activity logic to identify each activity that is ready to run on the processor.

23. *(Previously Presented)* An activity scheduler arranged to control activities in a plurality of processors, comprising:

a separate integrated circuit to support shared data and multi-tasking for each of said processors,

each integrated circuit being configured to support a control node mechanism comprising a set of stim-wait channels,

each stim-wait channel incorporating holding means to hold a pair of control variables for one of said activities, and

each of said separate integrated circuits further incorporating next activity logic to identify each activity that is ready to run on the associated processor.

24. *(Previously Presented)* An activity scheduler arranged directly to support shared data and multi-tasking in a network of processors, comprising:

a separate integrated circuit to support each of said processors,

each integrated circuit being configured to control a control node mechanism comprising a set of stim-wait channels,

each stim-wait channel incorporating holding means to hold a pair of control variables for one of said activities, and

each of said separate integrated circuits further incorporating next activity logic to identify each activity that is ready to run on the associated processor.

25. *(Previously Presented)* An activity scheduler, as in Claim 24, in which at least one of said processors is arranged to set at least one control variable in one of said separate integrated circuits.

26. *(Previously Presented)* An activity scheduler, as in Claim 24, including a peripheral device arranged to set at least one control variable in one of said separate integrated circuits.

27. *(Previously Presented)* An activity scheduler, as in Claim 24, in which at least one of said separate integrated circuits is arranged to set at least one control variable in another of said separate integrated circuits.

28. *(Previously Presented)* An activity scheduler, as in Claim 24, in which at least one control node mechanism has its set of stim-wait channels arranged as an array comprising n rows and m columns, and at least one of said separate integrated circuits is configured to support said array of control node mechanisms.

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29. *(Previously Presented)* An activity scheduler, as in Claim 24, in which the control variables are Boolean.

30. *(Previously Presented)* An activity scheduler, as in Claim 24, including inhibitor means operable to inhibit any changes to control variables from entering the next activity selection logic.

31. *(Previously Presented)* An activity scheduler, as in Claim 24, incorporating decoding and encoding logic to identify one or more of said activities and to route signals from said activity scheduler to the appropriate stim-wait channel.

32. *(Previously Presented)* An activity scheduler, as in Claim 24, including activity selection means operable to select the next activity on a round robin basis.

33. *(Previously Presented)* An activity scheduler, as in Claim 24, including priority selection means to allocate different priorities to groups of activities and to select the next of said activities within a group on a round robin basis within that group.

34. *(Currently Amended)* An activity scheduler, as in Claim 24, including a priority detector to detect an activity having a priority higher that the priority of an activity being processed on one of said processors, the priority detector being ~~arrange~~arranged to generate an interrupt signal to interrupt processing of the lower priority activity in favour of the higher priority activity.

35. *(Previously Presented)* An activity scheduler, as in Claim 22, in which the control variables are Boolean.

36. *(Previously Presented)* A method of controlling activities in a processor comprising holding a pair of control variables in respect of each activity, identifying the next activity to be run on the processor, and selecting the pair of control variables associated with the said next activity.

37. *(Previously Presented)* A method of controlling activities in a plurality of processors comprising holding a pair of control variables in respect of each activity in each processor, identifying the next activity to be run on each processor, and selecting the pairs of control variables associated with the next activity of each processor.

38. *(Previously Presented)* A processing network responsive to an activity scheduler as in claim 23.

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39. *(Previously Presented)* A processing network responsive to an activity scheduler as in claim 2.

40. *(Previously Presented)* A processing network as in claim 38, further comprising at least one peripheral device for setting at least one control-variable in said integrating circuit.

41. *(Previously Presented)* A processing network as in claim 39, further comprising at least one peripheral device for setting at least one control-variable in said integrating circuit.